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SIDLEY AUSTIN BROWN & WOOD LLP 717 NORTH HARWOOD SUITE 3400 DALLAS, TX 75201			FOWLKES, ANDRE R	
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			2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/858,396

Applicant(s)

CHEAH ET AL.

Examiner

Andre R. Fowlkes

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/11/05.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to the amendment filed 10/11/05.
2. Claims 1-41 are pending. Claims 1, 7, 19, 24 & 25 have been amended.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6, 13-24 and 30-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg U.S. Patent No. 4,607,332 in view of Maebayashi et al. (Maebayashi) U.S. Patent No. 5,450,589.

As per claim 1, Goldberg discloses **a method for providing data to an electronic device from a memory module, comprising the steps of:**

- reading said random access memory to determine whether said data is located in said nonvolatile reprogrammable memory (col. 1: 64 – col. 2: 4, "searches (i.e. reads) a RAM-located data structure ... the location of the replacement routine (i.e. data) is also found in the (RAM-located) data structure"),

- reading said read only memory, if said data is not located in said **nonvolatile reprogrammable memory** (col. 1:64-68 , "If there exists a correspondence between information passed on the call to the processing routine and certain elements of the data structure, a RAM based program is substituted for the ROM based program, (otherwise, the ROM based program is read)"),

-said update data thus provided to said electronic device being most recent **data** (col. 1:7-11 , "This invention relates ... to a method of dynamically altering firmware programs (with updated data, corresponding to fixed data) during execution of theses programs").

Although Goldberg system discloses the use of RAM and ROM, Goldberg doesn't explicitly disclose that the electronic device includes a **distinct nonvolatile reprogrammable memory**.

However, Maebayashi, in an analogous environment discloses that the electronic device has includes a **distinct nonvolatile reprogrammable memory**, (See Maebayashi, figure 4, EEPROM, 54).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have a **distinct nonvolatile reprogrammable memory**. The modification would have been obvious because one of ordinary skill in the art would have wanted to use the advantages of nonvolatile reprogrammable memory in addition

to the advantages of the RAM and ROM memories, together, to improve the speed and access time of the combined memory system.

Goldberg doesn't explicitly disclose **reading said nonvolatile reprogrammable memory, if said data is located in said nonvolatile reprogrammable memory, and wherein said nonvolatile reprogrammable memory contains updated data corresponding to fixed data contained in said read only memory.**

However, Maebayashi, in an analogous environment discloses **reading said nonvolatile reprogrammable memory, if said data is located in said nonvolatile reprogrammable memory, wherein said nonvolatile reprogrammable memory contains updated data corresponding to fixed data contained in said read only memory**, (col. 3:55-57, "Fig. 6 is a diagram showing ... the modification data (i.e. update modules) stored in the EEPROM (i.e. nonvolatile reprogrammable memory)").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have **reading said nonvolatile reprogrammable memory, if said data is located in said nonvolatile reprogrammable memory, wherein said nonvolatile reprogrammable memory contains updated data corresponding to fixed data contained in said read only memory.** The modification would have been obvious because one of ordinary skill in the art would have wanted to store and use data in nonvolatile reprogrammable memory in order to gain speed advantages while protecting the data from loss in the event of a power disconnection.

Goldberg doesn't explicitly disclose **accepting from said electronic device a request for said data**.

However, Maebayashi, in an analogous environment discloses **accepting from said electronic device a request for said data** (col. 8:12-15, "The processor ... may transfer the modification data to the adapters (requesting electronic device) ... only when the processor receives a request to transfer").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have **accepting from said electronic device a request for said data**. The modification would have been obvious because one of ordinary skill in the art would have wanted to control the flow of data using the well known and well documented request-response protocol.

As per claim 2, the rejection of claim 1 is incorporated and further, Goldberg discloses that **said random access memory is nonvolatile** (col. 1:53, "systems employing (nonvolatile or volatile) RAM").

As per claim 3, the rejection of claim 1 is incorporated and further, Goldberg discloses that **said nonvolatile reprogrammable memory contains the respective locations of said fixed data and said corresponding updated data** (col. 1: 64 – col.

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2: 4, "searches a RAM-located (i.e. nonvolatile reprogrammable memory) data structure (for the respective locations of said fixed data and said corresponding updated data)").

As per claim 4, the rejection of claim 3 is incorporated and further, Goldberg discloses that **said random access memory is volatile, said method further comprising the steps of: reading said nonvolatile reprogrammable memory to determine said respective locations; and updating said random access memory with said respective locations** (col. 1:53, "systems employing (nonvolatile or volatile) RAM", when volatile RAM is used, the data structure, containing the locations of the updated code, is transferred between nonvolatile reprogrammable memory and RAM).

As per claim 5, the rejection of claim 1 is incorporated and further, Goldberg doesn't explicitly disclose **displaying at least one of said fixed data and said updated data so as to allow said at least one of said fixed data and said updated data thus displayed to be modified; and storing the thus modified data in said nonvolatile reprogrammable memory as updated data.**

However, Maebayashi, in an analogous environment, discloses **displaying at least one of said fixed data and said updated data so as to allow said at least one of said fixed data and said updated data thus displayed to be modified; and storing the thus modified data in said nonvolatile reprogrammable memory as updated data** (col. 1:65-68, "a fixed program data storing unit for storing (and displaying) fixed program data; a modification data storing unit for storing (and

displaying) modification data (i.e. update data)", and col. 7:13-14, the system "write(s) (the updated) data in EEPROM").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have a the fixed and updated data displayed to be modified. The modification would have been obvious because one of ordinary skill in the art would have wanted to view the proposed modifications to confirm that they are desired.

As per claim 6, the rejection of claim 1 is incorporated and further, Goldberg doesn't explicitly disclose that **said nonvolatile reprogrammable memory is selected from the group consisting of: a flash memory; and an electrically erasable programmable read-only memory.**

However, Maebayashi, in an analogous environment, discloses that **said nonvolatile reprogrammable memory is selected from the group consisting of: a flash memory; and an electrically erasable programmable read-only memory** (col. 7:13-14, the system "write(s) modification data in EEPROM (or flash memory)").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have the nonvolatile reprogrammable memory selected from either flash memory or EEPROM. The modification would have been obvious because one of ordinary skill in the art would want the option of selecting the most appropriate the nonvolatile reprogrammable memory for each occasion.

As per claim 13, Goldberg discloses **a method for providing data to an electronic device, comprising the steps of:**

- creating said read only memory containing a first set of software modules; storing in said nonvolatile reprogrammable memory a second set of software modules, at least one module in said second set corresponding to a module in said first set (col. 1:7-11 , "This invention relates ... to a method of dynamically altering firmware programs (i.e. a 1st set of software modules located on a ROM) (with a 2nd set of software modules, corresponding to fixed data) during execution of theses programs").

- storing in said random access memory location information corresponding to said modules in said first and second sets (col. 1: 64 – col. 2: 4, "searches a RAM-located data structure (for the respective locations of the 1st and 2nd sets of modules)").

- storing in said random access memory a sequence of execution of selected ones of said modules in said first and second sets (col. 1: 64 – col. 2: 4, "searches a RAM-located data structure (for the respective locations of the 1st and 2nd sets of modules)" and the 2nd (i.e. updated) set of modules contains calls to execute a sequence of modules).

Goldberg doesn't explicitly disclose that the electronic device has **at least three distinct memories: a random access memory, a nonvolatile reprogrammable memory and a read only memory.**

However, Maebayashi, in an analogous environment discloses that the electronic device has **at least three distinct memories: a random access memory, a nonvolatile reprogrammable memory and a read only memory**, (See Maebayashi, figure 4).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have three distinct memories: a RAM, a ROM, and nonvolatile reprogrammable memory. The modification would have been obvious because one of ordinary skill in the art would have wanted to use the advantages of each memory type, in concert, to improve the speed and access time of the combined memory system.

As per claim 14, the rejection of claim 13 is incorporated and further, Goldberg discloses that **at least one module in said second set is an updated version of the corresponding module in said first set, said at least one module in said second set correcting an error in said corresponding module in said first set** (col. 1:7-25 , "This invention relates ... to a method of dynamically altering firmware programs (i.e. a 1st set of software modules located on a ROM) (with a 2nd set of software modules, corresponding to errors in the 1st set of software modules)").

As per claims 15-24, this is a memory module version of the claimed method discussed above, in claims 1, 2, 4-6 and 13, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Goldberg's dynamic alteration of firmware programs in read-only memory based systems (col. 1:7-2:4) and Maebayashi's firmware modification system (col. 1:65-7:14).

As per claim 30, this is a memory module version of the claimed method discussed above, in claims 2 and 4-6, wherein the disclosed communication technique has also been addressed and/or cited as set forth above. For example, see Goldberg's dynamic alteration of firmware programs in read-only memory based systems (col. 1:7-2:4) and Maebayashi's firmware modification system (col. 1:65-7:14).

Goldberg doesn't explicitly disclose using a first (communication subsystem) and second (base subsystem) memory subsystem, each containing a processor.

However, Maebayashi, in an analogous environment, discloses using a first (communication subsystem) and second (base subsystem) memory subsystem (Fig. 3, Processor 40.1 and processor 40.2, and associated text, e.g. 6:16-54).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have use a first and second memory subsystem. The modification would have been obvious because one of ordinary skill in the art would have wanted to use multiple processors to gain the speed and redundancy (i.e. fault resiliency) advantages.

As per claims 31-35, this is a memory module version of the claimed method discussed above, in claims 2 and 4-6, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Goldberg's dynamic alteration of firmware programs in read-only memory based systems (col. 1:7-2:4) and Maebayashi's firmware modification system (col. 1:65-7:14).

As per claim 36, this is a system version of the claimed method discussed above, in claims 5, 6 and 30, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Goldberg's dynamic alteration of firmware programs in read-only memory based systems (col. 1:7-2:4) and Maebayashi's firmware modification system (col. 1:65-7:14).

4. Claims 7-12 & 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg, U.S. Patent no. 4,607,332, in view of Maebayashi et al. (Maebayashi) U.S. Patent No. 5,450,589, further in view of Cole, U.S. Patent no. 6,074,434.

As per claim 7, Goldberg discloses **a method for providing data an electronic device from a memory module, comprising the steps of:**

-reading said random access memory to select an updated version of data stored in said nonvolatile reprogrammable memory and said read only memory, reading said updated version from said memory, and providing said updated

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version to said electronic device (col. 1: 64 – col. 2: 4, “searches a RAM-located data structure ... the location of the replacement routine is also found in the (RAM-located) data structure”, and col. 2: 2-4 “the processing routine effects a transfer to the replacement routine (located in nonvolatile reprogrammable memory)”).

Goldberg doesn't explicitly disclose that the electronic device has **at least three distinct memories: a random access memory, a nonvolatile reprogrammable memory and a read only memory.**

However, Maebayashi, in an analogous environment discloses that the electronic device has **at least three distinct memories: a random access memory, a nonvolatile reprogrammable memory and a read only memory**, (See Maebayashi, figure 4).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have three distinct memories: a RAM, a ROM, and nonvolatile reprogrammable memory. The modification would have been obvious because one of ordinary skill in the art would have wanted to use the advantages of each memory type, in concert, to improve the speed and access time of the combined memory system.

Goldberg doesn't explicitly disclose **accepting from said electronic device a request for said data.**

However, Maebayashi, in an analogous environment discloses **accepting from said electronic device a request for said data** (col. 8:12-15, "The processor ... may transfer the modification data to the adapters (requesting electronic device) ... only when the processor receives a request to transfer").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the system of Goldberg to have **accepting from said electronic device a request for said data**. The modification would have been obvious because one of ordinary skill in the art would have wanted to control the flow of data using the well known and well documented request-response protocol.

The Goldberg/Maebayashi combination doesn't explicitly disclose reading a memory to select a desired version of said data **from among a plurality of versions of said data** stored in a memory.

However, Cole, in an analogous environment, discloses reading a memory to select a desired version of said data **from among a plurality of versions of said data** stored in a memory (col. 2: 7-18, "a list of code updates (is read from a memory, and) ... a user ... may select from the list),

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Cole into the Goldberg/Maebayashi combination to have the user select from a plurality of versions of data. The modification would have been obvious because one of ordinary skill in the art

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would have wanted the ability to conveniently select a desirable data update version (Cole, col. 1:46-60).

As per claim 8, Goldberg also discloses such claimed limitations as addressed in claim 2 above.

As per claim 9, the rejection of claim 7 is incorporated and further, Goldberg discloses that **said nonvolatile reprogrammable memory contains respective locations of said plurality of versions** (col. 1: 64 – col. 2: 4, “searches a RAM-located data structure (for the respective locations of said fixed data and said corresponding updated versions)”).

As per claims 10-12, the Goldberg/Maebayashi/Cole combination also discloses such claimed limitations as addressed in claims 4, 9 and 6, above respectively.

As per claims 25-28, the Goldberg/Maebayashi/Cole combination also discloses such claimed limitations as addressed in claims 9, 2, 4 and 6 above, respectively.

5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg, U.S. Patent no. 4,607,332 in view of Cole, U.S. Patent no. 6,074,434, further in view of Maebayashi et al. (Maebayashi) U.S. Patent No. 5,450,589.

As per claim 29, the rejection of claim 1 is incorporated and further, the Goldberg/Cole combination doesn't explicitly disclose that **said nonvolatile reprogrammable memory is selected from the group consisting of: a flash memory; and an electrically erasable programmable read-only memory.**

However, Maebayashi, in an analogous environment, discloses that **said nonvolatile reprogrammable memory is selected from the group consisting of: a flash memory; and an electrically erasable programmable read-only memory** (col. 7:13-14, the system "write(s) modification data in EEPROM (or flash memory)").

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Maebayashi into the Goldberg/Cole combination to have the nonvolatile reprogrammable memory selected from either flash memory or EEPROM. The modification would have been obvious because one of ordinary skill in the art would want the option of selecting the most appropriate the nonvolatile reprogrammable memory for each occasion.

6. Claims 37-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goldberg U.S. Patent No. 4,0607,332 in view of Schurecht et al. (Schurecht) U.S. Patent No. 6,260,157.

As per claim 37, the rejection of claim 36 is incorporated and further, Goldberg doesn't explicitly disclose a **second data link for communicating with a communications service provider.**

However, Schurecht, in an analogous environment discloses a **second data link for communicating with a communications service provider** (col. 2:2, "a cellular telephone handset", and described further in reference to figure 1 in col. 3:65 – col. 5:42).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Schurecht into the system of Goldberg to have a data link for communicating with a communications service provider. The modification would have been obvious because one of ordinary skill in the art would have wanted to allow for bugs in the released code to be fixed/upgraded, via a wireless data link, without having to physically recall the product, (Schurecht, col. 2:32-48).

As per claim 38, the rejection of claim 37 is incorporated and further, Goldberg discloses **providing said updated data to said nonvolatile reprogrammable memory** (col. 2: 2-4 "the processing routine effects a transfer to the replacement routine (located in nonvolatile reprogrammable memory)").

Goldberg doesn't explicitly disclose that **the communications service provider is adapted to communicate with said base microprocessor via said second data link to provide said updated data to said nonvolatile reprogrammable memory.**

However, Schurecht, in an analogous environment discloses that the **communications service provider is adapted to communicate with said base microprocessor via said second data link to provide said updated data to said**

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nonvolatile reprogrammable memory (col. 2:2, "a cellular telephone handset", and described further in reference to figure 1 in col. 3:65 – col. 5:42).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Schurecht into the system of Goldberg to have **the communications service provider adapted to communicate with said base microprocessor via said second data link** to provide said updated data to said nonvolatile reprogrammable memory. The modification would have been obvious because one of ordinary skill in the art would have wanted to allow for bugs in the released code to be fixed/upgraded, via a wireless data link, without having to physically recall the product, (Schurecht, col. 2:32-48).

As per claim 39, this is a product version of the claimed system discussed above in claims 30 and 38, wherein all claimed limitations also have been addressed above and such a product is deemed to be inherent in the Goldberg/Schurecht system, otherwise it would be inoperative.

As per claims 40 and 41, Goldberg also discloses such claimed limitations as addressed in claim 1, above.

Response to Arguments

7. Applicants arguments have been considered but they are not persuasive.

In the remarks, the applicant has argued substantially that:

1) The proposed combination of Goldberg and Maebayashi would require a significant change in the principles of operation of one or both references; therefore, there can be no motivation to combine Goldberg and Maebayashi, at p. 13:1-10.

Examiner's response:

1) In response to applicant's argument that the proposed combination of Goldberg and Maebayashi would require a significant change in the principles of operation of one or both references, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In this case the Maebayashi reference is used to disclose using a non-volatile reprogrammable memory in addition to the RAM and ROM memories used by Goldberg, in a system to update firmware. One of ordinary skill in the art, at the time the invention was made would have found motivation to use these well-known and well-document technologies to create an efficient system by using the most advantageous type of memory in the part of the system where it's advantages can be used the most. Moreover, the plain language of the claim merely calls for having at least three distinct memories: RAM, ROM and non-volatile reprogrammable memory. It should be noted

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that the Goldberg system already uses RAM and ROM, so minimal alteration would be required. Therefore, applicant's argument is not persuasive.

In the remarks, the applicant has argued substantially that:

2) There is no disclosure that a processor or other device accepts a request for data from an electronic device or provides the data to the requesting electronic device, at p. 13:20-23, 14:17-19, 15:23-25 & 16:3-5.

Examiner's response:

2) The examiner disagrees with applicant's characterization of the applied art. Maebayashi discloses that a processor or other device accepts a request for data from an electronic device or provides the data to the requesting electronic device at col. 8:12-15, "The processor ... may transfer the modification data to the adapters (requesting electronic device) ... only when the processor receives a request to transfer".

In the remarks, the applicant has argued substantially that:

3) The applied art does not disclose a structure of first (communication subsystem) and second (base subsystem) memory subsystems including respective first and second processors adapted to communicate as recited in the claim, at p. 14:25-29, 15:10-15 and 17:5-10.

Examiner's response:

3) The examiner disagrees with applicant's characterization of the applied art. Maebayashi discloses using a first (communication subsystem) and second (base subsystem) memory subsystem at Fig. 3, Processor 40.1 and processor 40.2, and associated text, e.g. 6:16-54.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre R. Fowlkes whose telephone number is (571)

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272-3697. The examiner can normally be reached on Monday - Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ARF



TUAN DAM
SUPERVISORY PATENT EXAMINER